ABSTRACT OF THE DISCLOSURE

In fabrication of a nonvolatile memory cell having two floating gates, one or more peripheral transistor gates are formed from the same layer (140) as the select gate. The gate dielectric (130) for these peripheral transistors and the gate dielectric (130) for the select gates are formed simultaneously. In a nonvolatile memory having a memory cell with two floating gates, the gate dielectric (130) for the peripheral transistors and the gate dielectric (130) for the select gates (140) have the same thickness.